ELECTRONIC DEVICE AND METHOD FOR FABRICATING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

The present application claims priority of Korean Patent Application No. 10-2014-0024043, entitled "ELECTRONIC DEVICE AND METHOD FOR FABRICATING THE SAME" and filed on Feb. 28, 2014, which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

This patent document relates to memory circuits or devices and their applications in electronic devices or systems.

BACKGROUND

Recently, as electronic devices or appliances trend toward miniaturization, low power consumption, high performance, multi-functionality, and so on, there is a demand for electronic devices capable of storing information in various electronic devices or appliances such as a computer, a portable communication device, and so on, and research and development for such electronic devices have been conducted. Examples of such electronic devices include electronic devices which can store data using a characteristic switched between different resistant states according to an applied voltage or current, and can be implemented in various configurations, for example, an RRAM (resistive random access memory), a PRAM (phase change random access memory), an FRAM (ferroelectric random access memory), an MRAM (magnetic random access memory), an E-fuse, etc.

SUMMARY

The disclosed technology in this patent document includes memory circuits or devices and their applications in electronic devices or systems and various implementations of an electronic device, in which an electronic device may include a transistor having an excellent characteristic and a semiconductor memory having the transistor and a method of fabricating the same.

In one aspect, an electronic device is provided to include a transistor that includes a gate where at least a portion of the gate is filled in a semiconductor substrate including an active region defined by an isolation layer; a junction which is disposed over the active region at both side of the gate and includes a metal-containing layer and a first semiconductor layer doped with an impurity and interposed between the active region and the metal-containing layer; and a material layer which is interposed between the junction and the active region to prevent diffusion of the impurity from the first semiconductor layer and defines an opening for coupling the junction to the active region. In another aspect, an electronic device is provided to include a transistor that includes a substrate including an active region and an isolation layer which defines the active region; a gate formed on the substrate to include at least a portion of the gate which is filled in the substrate; a junction which is disposed over the active region at both sides of the gate and includes a metal-containing layer and a first semiconductor layer doped with an impurity and interposed between the active region and the metal-containing layer; and a material layer which is interposed between the junction and the active region to prevent diffusion of the impurity from the first semiconductor layer and defines an opening for coupling the junction to the active region.

In some implementations, top surface of the first semiconductor layer is lower than a top surface of the gate. In some implementations, a thickness of the first semiconductor layer is smaller than a thickness of the metal-containing layer. In some implementations, the material layer includes a material which applies a stress to a channel of the transistor. In some implementations, the material layer includes a silicon nitride. In some implementations, the transistor further comprises a metal-semiconductor compound layer interposed between the first semiconductor layer and the metal-containing layer. In some implementations, the transistor further comprises a second semiconductor layer which is formed in the opening and is positioned at a same level as the material layer in a vertical direction. In some implementations, the second semiconductor layer is an epitaxial semiconductor layer. In some implementations, a concentration of the impurity of the first semiconductor layer is higher than that of the second semiconductor layer or the active region. In some implementations, a top surface of the active region is higher than a top surface of the isolation layer in a region where the gate is formed. In some implementations, the electronic device further comprises a memory element which is coupled to the junction disposed at one side of the gate. In some implementations, the memory element includes a variable resistance element which is switched between different resistant states according to an applied voltage or current. In some implementations, the variable resistance element includes a first magnetic layer, a second magnetic layer and a tunnel barrier layer interposed between the first magnetic layer and the second magnetic layer

In some implementations, the electronic device may further include a microprocessor which includes: a control unit configured to receive a signal including a command from an outside of the microprocessor, and performs extracting, decoding of the command, or controlling input or output of a signal of the microprocessor; an operation unit configured to perform an operation based on a result that the control unit decodes the command; and a memory unit configured to store data for performing the operation, data corresponding to a result of performing the operation, or an address of data for which the operation is performed, wherein the transistor is part of at least one of the control unit, the operation unit and the memory unit in the microprocessor.

In some implementations, the electronic device may further include a processor which includes: a core unit configured to perform, based on a command inputted from an outside of the processor, an operation corresponding to the command, by using data; a cache memory unit configured to store data for performing the operation, data corresponding to a result of performing the operation, or an address of data for which the operation is performed; and a bus interface connected between the core unit and the cache memory unit, and configured to transmit data between the core unit and the cache memory unit, wherein the transistor is part of at least one of the core unit, the cache memory unit and the bus interface in the processor.

In some implementations, the electronic device may further include a processing system which includes: a processor configured to decode a command received by the processor and control an operation for information based on a result of decoding the command; an auxiliary memory device configured to store a program for decoding the command and